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EXAMINER	
KNAUSS, SCOTT A	

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,541	ROBERT ET AL.	
	Examiner	Art Unit	
	Scott Alan Knauss	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-12* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/936,951.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The references cited in the information disclosure statement have been considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1,2,6,9,10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,367,593 (Lebby et al) in view of US 5,923,691 (Sato)

Regarding claim 1, Lebby discloses in figs. 2 and 3 and the accompanying description:

An optoelectronic connector comprising:

An optical port #32

An electrical port #40

An optoelectronic circuit #50 positioned in the package and connected to the optical and electrical ports

An internal wall #30 of the package being provided with metallized connections, pads of an IC chip #50 being connected directly to the metallized connections (via solder bumps #39 (see col. 3, lines 32-37, the "pads" being the part of the chip in contact with the solder bumps)

The device can also be considered a "base unit" link, as it can be used to transmit and receive signals from a fiber optic cable #47, thus serving as a "base" for communication with the fiber optic cable.

Lebby further discloses the use of an IC chip #50 which is placed in well #30, and can be considered to be a "bare" chip, because it is placed directly into the well #30 without an intermediate package in which it is contained.

Furthermore, Lebby discloses that photonics components may comprise both light receiving and light emitting elements (col. 3, lines 6-10), thus the chip #50 can be considered be an emission (light emitting) and detection (light detecting) IC chip.

Although Lebby does not explicitly specify using the IC chip to *control* the emission-detection elements, such an arrangement is well known in the art, for

example, to amplify optical signals received using amplifier circuitry on an IC chip, and to drive optical transmitting elements via the IC chip

Therefore it would have been obvious to one of ordinary skill in the are to modify the optoelectronic connector of Lebby to use amplifier or driver circuitry on the IC chip #50 in order to drive optical transmitters or amplify optical signals received via the IC chip, and thus control the emission detection elements.

Lebby does not disclose the material from which the diodes are formed, in particular, the use of GaAs substrate. However, the use of GaAs is well known in the art as a substrate material for laser diodes. One example of this is shown by Sato in fig. 5 and col. 8, lines 38-40, which utilizes a GaAs substrate in formation of a VCSEL laser diode. Therefore, since the use of such materials for substrates of laser diodes is well known in the art, one of ordinary skill in the art would have been motivated to use known materials in fabricating the laser diodes of Lebby, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use, in this case, for formation of a VCSEL laser diode to transmit light.

Lebby does not disclose the process limitations of:

"the laser diodes being formed in a predetermined arrangement from a gallium arsenide substrate and deposited on the IC chip by transfer from an intermediate support that maintains the predetermined arrangement.

Instead, Lebby discloses that photonic components, which may include laser diodes (vertical cavity surface emitting lasers, which are a type of laser diodes, col. 3, lines 6-10) may be formed directly on an IC chip (col. 4, lines 42-43), but does not disclose how they are placed there.

However, according to MPEP 2113:

"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."

The applicant has set forth arguments in the parent application 09/936,951, dated 11/17/03 regarding what was then claim 33, that this process results in improved tolerances on laser diode locations, and reduction or elimination of faults in other components arising from conventional techniques (page 10 of response)

However, the examiner is not convinced by these arguments. The examiner does not find the features of improved tolerances and lack of damage to other components to structurally distinguish applicant's invention from the prior art. The examiner submits

that it is well known in the art to form components on a chip in a highly precise manner to facilitate their alignment with other components, and it is unclear from applicant's specification and remarks why such a process would necessarily result in better positioning of the diodes, furthermore, in order to successfully fabricate a working device of the type disclosed by Lebby, it would further have been obvious to fabricate the diodes on the chip without damaging other components on the chip, otherwise, the device would not work properly.

It is the examiner's opinion that the arguments and specification of the current application do not sufficiently distinguish the structure of the current invention from the prior art. The examiner believes that it would have been obvious to one of ordinary skill in the art to place diodes on the chip in a highly precise manner, without damaging other components, for the purpose of providing precise alignment between the laser diodes and the components to which they are optically connected to, thus providing a low loss connection, and it would further have been obvious to place the diodes in such a way that faults in the other components on the chip are prevented, for the purpose of providing a device which works correctly.

Applicant also argued that Lebby does not disclose laser diodes formed on a bare integrated circuit chip (page 8 of response), However the examiner believes that since Lebby discloses photonic components formed directly on the chip, which may include laser diodes (VCSEL's), and further discloses placing the chip directly into a well of the

device without any intermediate packaging for the chip, Lebby can be considered to disclose a chip which is "bare" (i.e. unpackaged) with the laser diodes formed thereon.

Regarding claim 2, Lebby fails to disclose the laser diodes being placed on the substrate with a space between the diodes equal to a space between optical fiber terminations in the optical port.

Nevertheless, it is well known in the art to precisely align a fiber and a laser diode to maximize the in-coupling of light to the fiber. As such, it would have been obvious to one of ordinary skill in the art to match the spacing of photonic components #45 (which may include laser diodes) to the spacing of fiber terminations #47, for the purpose of ensuring efficient coupling between the laser diodes and the fiber terminations #47.

Regarding claim 6, Lebby, as modified by Sato above, discloses the use of VCSEL diodes, which may be made of GaAs material as disclosed by Sato.

Regarding claim 9, Lebby discloses an optical port which has access limited to the number of optical ports available, and discloses the use of at least two optical channels (disclosing a plurality of fibers #47). Lebby further discloses a plurality of contacts #40, but does not disclose the use of contacts for electrical signals and contacts for a ground signal.

Nevertheless, in electrical circuits, it is well known that any integrated circuit will need to be connected to both electrical signals (input/output) as well as a ground signal, for the purpose of providing electrical power to the circuit.

Therefore it would have been obvious to one of ordinary skill in the art to supply IC #50 with both ground and electrical signals for the purpose of supplying electrical power to the IC.

Regarding claim 10, the flat upper and lower surfaces of connector #25 can be considered means for stacking individual connectors (which can be considered modules)

Regarding claim 12, the connector of fig. 2 is designed to convert signals between electrical conductors #40 and optical conductors #47.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lebby in view of Sato as set forth above, and further in view of US 5,675,685 (Fukuda et al)

Regarding claim 11, Lebby discloses laser diodes formed on an IC chip, but does not disclose whether connection wires are used to connect between pads of the diodes and pads of the IC chip.

Nevertheless, it is well known to use wire connections to connect between a laser diode and an IC. One example of this is shown by Fukuda in fig. 1, which discloses the use of wire bonds #13in order to connect laser diodes #1 to IC #2, the wires inherently being connected to some sort of pad on both the diode and the IC. Therefore it would have been obvious to one of ordinary skill in the art to use known connection methods, including the use of connection wires as taught by Fukuda for the purpose of providing electrical connection between laser diodes and the IC of Lebby.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1,3-5 and 7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1,2,4 and 5 of U.S. Patent No. 6,758,606. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim 1 of the '606 patent discloses all the limitations of claim 1 of the application, including a package, optical and electrical ports, an optoelectronic circuit with a bare control and emission detection IC chip, an internal wall having metallized connections, pads of the integrated circuit being connected to the metallized connections. The patent also discloses in claim 1 laser diodes being laid out on (and thus formed from) a GaAs substrate, and being transferred (and thus deposited on) to the IC chip via an intermediate support. The patent does not, however disclose the diodes being formed in a predetermined arrangement on the IC chip or the predetermined support.

Nevertheless, it is well known in optoelectronic devices that light emitting and receiving elements must be accurately placed on a substrate in order to align them with other optical devices. As such, one of ordinary skill in the art would have been motivated to ensure that the diodes are maintained in a particular predetermined arrangement both on the intermediate support and the IC chip, for the purpose of forming an optoelectronic device which accurately aligns the laser diodes with optical elements (such as waveguides) with which they communicate.

Claim 1 of the Patent also discloses additional details not claimed in the current application, in particular, the feature of the package being a MID package with connection metallizations. However, the examiner submits that merely providing a device with less structure would have been obvious to one of ordinary skill in the art in order to simplify the manufacturing process.

Regarding claims 3 and 5, claims 2 and 4 of the patent is substantially identical.

Regarding claim 4, the package in the '606 patent is a MID package (see claim 1) and is connected to the IC via BGA connections, wire bonding, or anisotropic film technology.

Regarding claim 7, claim 5 of the Patent discloses all the limitations of claim 1 as set forth above, except it has a 45 degree inclined mirror instead of a MID package.

Allowable subject matter

8. Claims 3-5 and 7 would be allowable if the Double Patenting rejection is overcome and the claims are rewritten in independent form including the limitations of the claims from which they depend. Prior art fails to teach or suggest a package as set

forth in claim 1, further comprising a package which is a MID package or has MID shielding. Regarding claim 7, the prior art fails to disclose a package as set forth in claim 1 incorporating a 45 degree inclined mirror.

9. Claim 8 is objected to for depending from a rejected base claim, but would be allowable if rewritten in independent form including the limitations of the claims from which it depends. Prior art fails to disclose the optical port comprising a part for positioning optical fiber terminations, this part abutting a cant (edge) of the IC.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Alan Knauss whose telephone number is (571) 272-2350. The examiner can normally be reached on 9-5 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sak